

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 35

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte RYOUHEI KIRISAWA,  
RIICHIRO SHIROTA,  
RYOZO NAKAYAMA,  
SEIICHI ARITOME,  
MASAKI MOMODOMI,  
YASUO ITOH,  
FUJIO MASUOKA

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Appeal No. 95-1536  
Application 07/746,176<sup>1</sup>

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HEARD: OCTOBER 13, 1998

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Before URYNOWICZ, JERRY SMITH and BARRETT, Administrative Patent Judges.

URYNOWICZ, Administrative Patent Judge.

DECISION ON APPEAL

This appeal is from the final rejection of claims 1-34, all the claims pending in the application.

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<sup>1</sup> Application for patent filed August 15, 1991.

The invention pertains to a non-volatile semiconductor memory device. Claim 1 is illustrative and reads as follows:

1. A non-volatile semiconductor memory device comprising:  
a semiconductive substrate;  
parallel bit lines provided above said substrate;  
memory cells connected to said bit lines, said memory cells comprising cell blocks each of which has a series array of memory cell transistors connected at a first node thereof to a corresponding bit line associated therewith and connected at a second node thereof to said substrate, each of said memory cell transistors having a carrier storage layer and a control gate electrode; and  
means for sequentially programming selected memory cell transistors in such a manner as to write a logical data into a certain memory cell transistor which is presently selected from said memory cell transistors by injecting carriers by tunneling into the carrier storage layer of said certain memory cell transistor thereby to increase a threshold value thereof, and for sequentially erasing the selected memory cell transistors in a manner as to erase the data stored in said certain memory cell transistor by removing the carriers accumulated in said carrier storage layer thereby to decrease the threshold value of said certain memory cell transistor.

The references relied upon by the examiner as evidence of obviousness are:

Momodomi et al. (Momodomi '812)	4,959,812	Sep. 25, 1990
Sumihiro (Japan, Kokai)	60-182162	Sep. 17, 1985
Momodomi et al. (Momodomi '900) (European Patent Application)	0 322 900	July 05, 1989

Adler, "Densely Arrayed EEPROM Having Low-Voltage Tunnel Write,"  
I.B.M. Technical Disclosure Bulletin, Volume 27, No. 6, Nov. 1984, pp. 3302-3307.

Masuoka et al. (Masuoka), "New Ultra High Density EPROM and Flash  
EEPROM with NAND Structure Cell," International Electron Devices  
Meeting Technical Digest, Dec. 6-9, 1987, pp. 552-555.

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Shirota et al. (Shirota), "A New NAND Cell for Ultra High Density 5V-Only EEPROMs," 1988 Symposium on VLSI Technology Digest of Technical Papers, San Diego, May 10-13, 1988, IEEE Cat. No. 88CH-2597-3, pp. 33-34.

Claims 1-34 stand rejected under 35 U.S.C. § 112, first and second paragraphs.

Claims 17, 18, 20 and 22 stand rejected under 35 U.S.C. § 102(a), (e) and/or (g) as anticipated by, or in the alternative, under 35 U.S.C. § 103 as obvious over Momodomi '812.

Claims 1-3 and 17-19 stand rejected under 35 U.S.C. § 103 as unpatentable over Adler in view of Sumihiro.

Claims 1-4, 6, 10 and 13-17 stand rejected under 35 U.S.C. § 103 as unpatentable over either of Shirota or Masuoka and Sumihiro taken together.

Claims 18-20 and 22 stand rejected under 35 U.S.C. § 103 as unpatentable over Masuoka in view of Sumihiro and Adler.

Claims 4, 5, 7-12, 17-19, 21, 23 and 25-34 stand rejected under 35 U.S.C. § 103 as unpatentable over Adler in view of Sumihiro and Shirota.

Claims 1-34 stand rejected under 35 U.S.C. § 102(a) as anticipated by, or in the alternative, under 35 U.S.C. § 103 as obvious over Momodomi '900.

The respective positions of the examiner and the appellants with regard to the propriety of these rejections are set forth in the final rejection of June 16, 1993 and the examiner's answer dated November 22, 1994, and the appellants' amended and reply briefs filed July 1, 1994 and January 23,

1995, respectively.

### Appellants' Invention

The invention is a non-volatile semiconductor memory device, and method for accessing data in a non-volatile semiconductor memory device. The embodiment of Figures 1-4 includes parallel bit lines BL1-BL8 provided on a semiconductor substrate. Memory cells M11...M88 are connected to the bit lines. The memory cells comprise cell blocks B1-B8, each of which has a series array of memory cell transistors connected at a first node QS11-QS81 to a corresponding bit line associated therewith and connected at a second node to the substrate Vs. Each of the memory cell transistors has a carrier storage layer 28 and a control gate electrode 32.

The memory includes a means for sequentially programming selected memory cell transistors to write data into a certain memory cell transistor by injection of carriers by tunneling into the carrier storage layer, and for sequentially erasing the selected memory cell transistors to erase the data stored in the certain memory cell transistor by removing the carriers accumulated in the charge storage layer.

A data erase operation involves applying a 20 volt pulse to a control gate line SG1. The selection transistor QS11 is rendered conductive, and cell block B1 is electrically connected with the corresponding bit line BL1. A potential of 20 volts is simultaneously applied to the bit line BL1 while zero volts is applied to the word lines WL1-WL8 in the M1 period of the illustrated

erasing cycle. A high-intensity electric field is formed between the floating gate 28 of memory cell M11 and the substrate 22. Thus, electrons which have accumulated in the floating gate 28 discharge to the substrate and the drain 42. As a result, the threshold value of the memory cell transistor M11 is shifted in the negative direction.

In the next cycle labeled M2 (Figure 7), the method is the same except that a 20 volt pulse is also applied to word line WL1 and the potential of the bit line is transferred to the drain layer of memory cell M12 through the first selection transistor QS11 and memory cell M11. Similar to memory cell M11, memory cell M12 is thus erased. The procedure is repeated by sequentially applying the high level voltages as illustrated in Figure 7 to the various word lines, thereby sequentially erasing the memory cells of cell block B1 in an order from M11 to M18.

In the data write cycle for memory cell M8 (Figure 9), a high level voltage is applied to control gate line SG1, rendering transistor QS11 conductive and electrically connecting the cell block B1 with the bit line BL1. An intermediate level potential voltage is applied to word lines WL1-WL7 while a high level voltage is applied only to word line WL8. A high intensity electric field is thus formed only between the floating gate of the selected memory cell M8 and the substrate 22, and a tunnel current flows therebetween. This process is repeated where a high level voltage is applied sequentially to memory cells M7-M1 through word lines WL7-WL1, thereby sequentially writing data into each of these memory cells.

Opinion

The Rejection under 35 U.S.C. § 112, First Paragraph:

We will not sustain this rejection. We find no merit to the examiner's position to the effect that appellants' disclosure is not enabling because it does not specifically disclose "means for sequentially programming selected memory cell transistors...and for sequentially erasing the selected memory cell transistors in a manner...". This language is directed to memory address circuitry for providing the disclosed pulses for addressing the transistor memory array. Circuitry for addressing the cells of memory arrays are notoriously old in the art, and the examiner has made no specific showing why it would not have been obvious for one of ordinary skill in the art to make the address circuitry for producing the pulses disclosed by appellants for operating their memory in the manner disclosed. An inventor need not explain every last detail of his invention since he is speaking to those skilled in the art and may rely on the skill in the art to provide the same. DeGeorge v. Bernier, 768 F.2d 1318, 1322, 226 USPQ2d 758, 762 (Fed. Cir. 1985).

The Rejection under 35 U.S.C. § 112, Second Paragraph:

We will not sustain this rejection. We find no merit to the position to the effect that use of the terms "program" and "erase" render the claims indefinite. Appellants recite programming selected memory cell transistors in such a manner as to write data. Programming is broadly setting a routine and

it is clear from appellants disclosure that this language is meant to cover the routine disclosed by appellants of writing data into memory cell transistors. The use of the term program or programming in relation to the function does not appear to confuse the meaning of the claims.

Appellants specifically disclose an erase function. Accordingly, when read in light of appellants' disclosure, one of ordinary skill in the art would have known what is meant in the claims by terminology such as "sequentially erasing the selected memory cell transistors".

Because appellants specifically disclose "H" and "L" level potentials in their specification, we find no merit to the position that signal levels referred to in the claims as "high", "H", "low" and "L" have no meaning and render the claims indefinite. Rather than recite specific signal levels, appellants have chosen to define their invention broadly by indicating the relative sizes of signals used in the invention.

Lastly, we find no merit to the examiner's criticism of appellants' use of the term "NAND" as having no meaning. At page 2, lines 6-14, appellants explain what constitutes a "NAND cell".

The Rejections over Prior Art:

After consideration of the positions and arguments presented by both the examiner and the appellants, we have concluded that none of the prior art rejections should be sustained. We agree in general with the comments made by appellants; we add the following discussion for emphasis.

All of the claims require sequential erasing of data from memory cells. None of the prior art references teaches sequential erasing. Rather, each of the references teaches simultaneous erasing of cells and, with the exception of Momodomi '812, the examiner has not tried to explain why one of ordinary skill in the art at the time the invention was made would have found it obvious to modify the prior art to use sequential erase of data cells. In re Fritch, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1783-1784 (Fed. Cir. 1992).

Although Momodomi '812 also teaches that data can be erased one byte at a time, this does not constitute the sequential erasure of data from individual memory cells. In discussing Momodomi '812 at page 11 of his answer, the examiner takes the position that simultaneous erasure requires a large power supply and that the sequential erasure of cells would have been obvious to permit the use of a smaller power supply and that only those areas desired to be erased would be erased. This is not persuasive. As noted by appellants, the examiner's assertion to the effect that sequential erasure would permit use of a smaller power supply is unsubstantiated. As further noted by appellants, the teachings of the reference at column 11, lines 27-32, that no high gate voltage is needed for erasing data and that the invention enables the reduction of the power dissipation in the EEPROM suggest that, contrary to the examiner's position, a large power supply is not needed in the prior art device.

The examiner takes the position that erasure of data in the prior art apparatus is only those cells in which one might desire to erase data suggests sequential erasure of data. Even assuming the erasure

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of data in less than all cells would have been obvious to one of ordinary skill in the art, the artisan would have been directed to simultaneous erasure of data as taught by the prior art of record, not sequential erasure of data.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

REVERSED

STANLEY M. URYNOWICZ, JR.	)	
Administrative Patent Judge	)	
	)	
	)	BOARD OF PATENT
	)	APPEALS AND
JERRY SMITH	)	INTERFERENCES
Administrative Patent Judge	)	
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	)	
LEE E. BARRETT	)	
Administrative Patent Judge	)	

SMU/dal

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Oblon, Spivak, McClelland,  
Maier & Neustadt  
1755 Jefferson Davis Hwy.  
Fourth Floor  
Arlington, VA 22202